IN THE TITLE

Please amend the title as follows:

SUBSTRATES AND SYSTEMS TO MINIMIZE ~~ARRANGEMENTS FOR MINIMIZING~~ SIGNAL PATH DISCONTINUITIES

IN THE SPECIFICATION

Please make the paragraph substitutions indicated below. The specific changes incorporated in the substitute paragraphs are shown in the following marked-up versions of the original paragraphs.

The paragraph beginning on page 1, line 19 is amended as follows:

As system frequency increases (e.g., from 533 MHz to 2.5 Gigabits/second) to meet performance demands, the effects of signal path deficiencies become more pervasive. Needed are arrangements to increase ~~minimize~~ signal integrity in the signal paths.

The paragraph beginning on page 8, line 1 is amended as follows:

Discussion turns now to the example dashed arrow path 430 of FIG. 4, such FIG. 4 omitting a number of FIG. 3 items for sake of simplicity/clarity. That is, an example signal may travel from an electrical component (not shown; e.g., motherboard) on which the substrate 110 is mounted, through the conductive bump/balls 160, to a land 370. In the FIG. 4 arrangement, the lands are located along the secondary-side external conductive build-up layer 350Q. The signal may further travel, from the land 370 onto another portion (e.g., a trace) of the secondary-side external conductive build-up layer 350Q, and then along one or more vias 360 on a secondary side of the substrate to travel through each of the layers 340D, 350P, 340C, 320Y, 310, 320X and 340B, to arrive at the layer 350N. The signal path 430 may then travel along a trace within the layer 350N onto another via 360, and from there, onto a portion (e.g., trace, land) of the layer 350M, and then onto the die 120.

The paragraph beginning on page 10, line 3 is amended as follows:

FIG. 5 is a side view 500 similar to that of FIG. 4, but showing an example embodiment of the present invention. This example embodiment provides a differently-arranged substrate

110', designed to attempt to minimize signal path discontinuities (e.g. variations in impedance). More particularly, the FIG. 5 embodiment has, for example, a core 310' and multiple build-up layers 320X', 340B', 350N' 340A', 350M' on the primary-side, and a lesser number of build-up layers, such as only one peripheral core conductive layer 320Y', on the substrate 110's secondary side (e.g., core bottom side). That is, the build-up layers 340C, 350P, 340D, 350Q that were present on the bottom side of the core 310 in the FIG. 4 arrangement have been reduced, or eliminated. Practice of embodiments of the present invention is not limited to this specific arrangement, and instead, other example embodiments may be where the substrate mounting-side of the arrangement has one-quarter, one-third or even one-half a number of conductive layers as opposed to a number of the primary-side of the package.

The paragraph beginning on page 13, line 6 is amended as follows:

In concluding, in such FIG. 5 example embodiment, there may occur a lesser variation between a mounting-component-side signal entering the bottom of the substrate 110, and the primary-side signal leaving the substrate to enter the die 120. While the example embodiment was described as reducing any [[an]] impedance and physical joint discontinuities at an input/output of a secondary side of the substrate 110', practice of the present invention can just as easily be applied to reduce discontinuities at an input/output of a primary (die) side, or even within internal layers of the substrate. For example, if a localized impedance discontinuity is determined to exist along an internal signal path as a result of parasitic capacitance between ones of the internal layers (e.g., neighboring vertical vias), modifications (e.g., increased separation distance; changing of a material there-between to one having a differing permittivity) may be used to reduce the localized impedance discontinuity to within a predetermined acceptable range.